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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER
TRINH, MICHAEL MANH

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 09/22/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/899,957	ADKISSON ET AL.	
	Examiner	Art Unit	
	Michael Trinh	2822	

-- The MAILING DATE of this communication appears on the cover sheet with th correspond nce address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 June 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *12-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *12-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

*** This office action is in response to Applicant's amendment and RCE filed on June 30, 2003. Claims 12-21 are currently pending.

*** The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 102

1. Claims 12-14,17-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Nowak et al (6,528,846).

Nowak teaches an asymmetric field effect transistor comprising: a semiconductor layer 7 formed on an insulator layer 2, wherein the semiconductor layer 7 including impurities supplied thereto and adjacent source and drain regions 39,41 (Figs 1D-1G), wherein the impurities in regions 21,31,24,23 have a location precisely defined by edges of the gate structure 15 having an oxide layer 17, and locate in portions of the semiconductor layer, and locate at edges of a trench formed by the dielectric layer 35; and a gate structure 15 formed on a portion of the semiconductor layer in the trench formed by the dielectric layer 35 with asymmetrical diode properties at the source and drain regions 39,41, wherein floating body effect of the transistor is reduced due to the electrical connection between the source and the floating body (col 1, lines 15-20; col 3, lines 20-26, lines 45-50). Re claims 13 and 17, wherein source and drain regions 39,41 are formed adjacent to the gate structure 15, and wherein there is no dielectric layer thereon (Fig 1G). Re claim 18, wherein the gate structure 15 is planarized to the dielectric layer 35. Re claims 14, 19, 20, and 21, Re further claims 12-21, the claims are directed to the product per se, no matter how actually made by process limitations including "implanting", "diffusion" from "a sidewall within", "angled implantation", "planarizing", "removing", etc..

A "product by process" claim is directed to the product per se, no matter how actually made, *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); In re Marosi et al, 218 USPQ 289; and particularly In re Thorpe, 227 USPQ 964, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a

new method is not patentable as a product, whether claimed in "product by process" claims or not.

2. Claims 12-14,17,19-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Long et al (6,525,381).

Long et al teach an asymmetric field effect transistor comprising: a semiconductor layer (e.g. 14 in Fig 2, col 4, line 45 through col 5; or 114 in Figs 8-11; col 6, line 54 through col 8) formed on an insulator layer 16 (Fig 2), wherein the semiconductor layer 14 including impurities supplied thereto and adjacent source and drain regions 20,22, wherein the impurities have a location precisely defined at edges of the gate structure 48, locate in portions of the semiconductor layer, and locate at edges of a trench formed by the dielectric layer 70/72; and a gate structure 48 formed on a portion of the semiconductor layer with asymmetrical diode properties at the source and drain regions 20,22 (Fig 2; col 1, lines 60-65), wherein the transistor is formed to avoid of floating body effect (col 1, lines 10-13), wherein the floating body effect is substantially avoided and reduced due to the electrical coupling between the source and the floating body (col 1, lines 1-13,40-50). Re claims 13 and 17, wherein source and drain regions 20,22 are formed adjacent to the gate structure 48, and wherein there is no dielectric layer thereon (Figs 1). Re further claims 12-14,17,19-21, the claims are directed to the product per se, no matter how actually made by process limitations including "implanting", "diffusion" from "a sidewall within", "angled implantation", "planarizing", "removing", etc..

A "product by process" claim is directed to the product per se, no matter how actually made, *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); In re Marosi et al, 218 USPQ 289; and particularly In re Thorpe, 227 USPQ 964, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not.

Claim Rejections - 35 USC § 103

3. Claims 15-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nowak et al (6,528,846) taken with Lee (6,214,677).

Nowak teaches an asymmetric field effect transistor as applied to claims 12-14,17-21 above.

Re claims 15-16, Nowak lacks to form a planarized insulator layer to the gate structure 213 as shown in Figure 4D.

However, Lee teaches (at col 3, lines 47-68; Figs 1C-1D) that after forming source and drain regions 122, deposit an oxide insulator layer and planarized to form the planarized oxide insulator layer 124 with the gate structure 116a (Fig 1D).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the transistor of Nowak by forming a planarized insulator layer on the gate structure as taught by Lee. This is because of the desirability to form a planar device structure, to protect the underlying structure, and to form an interlayer insulator for subsequent electrical connection.

4. Claims 15-16,18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Long et al (6,525,381) taken with Lee (6,214,677).

Long et al teach an asymmetric field effect transistor as applied to claims 12-14,17,19-21 above.

Re claims 15-16, Long et al lack to form a planarized insulator layer to the gate structure 213 as shown in Figure 4D. Re claim 18, the gate structure is planarized to the dielectric layer.

However, Lee teaches (at col 3, lines 47-68; Figs 1C-1D) that after forming source and drain regions 122, deposit an oxide insulator layer and planarized to form the planarized oxide insulator layer 124 with the gate structure 116a (Fig 1D). In another words, Lee teaches (at col 3, lines 47-68; Figs 1C-1D) depositing and planarizing an oxide dielectric layer to form a planarized oxide dielectric layer 124 so that the gate structure 116a is planarized with the dielectric layer 124 (Fig 1D).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the transistor of Long by forming a planarized insulator layer or

dielectric layer adjacent to the gate structure as taught by Lee. This is because of the desirability to form a planar device structure, to protect the underlying structure, and to form an interlayer insulator or dielectric layer for subsequent electrical connection.

5. Claims 20-21 are further rejected under 35 U.S.C. 103(a) as being unpatentable over Nowak et al (6,528,846) or Long et al (6,525,381) taken with Chau et al (5,434,093).

Nowak or Long teaches an asymmetric field effect transistor formed on a semiconductor substrate as applied to claims 12-14,17-19 above.

Nowak or Long teaches forming a doped region by implantation impurities, but lacks forming a sidewall of a doped material for diffusing impurities as recited in claims 20-21.

It is maintained that the claims are directed to the product per se, no matter how actually made by process limitations including impurities have been supplied by diffusion from the sidewall within the trench, In re Thorpe, 227 USPQ 964. Chau is however cited to show (at col 14, line 60 through col 15, line 30; Figs 5a-5d) a doped region 503b formed by diffusing impurities from a sidewall 510b of a doped material.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the transistor having the doped region of Nowak or Long by diffusing impurities from the sidewall of a doped material as taught by Chau, because these techniques are alternative and equivalent for substitution in order to the doped region at the edge of the gate structure.

Response to Arguments

6. Applicant's amendment and remarks filed June 30, 2003 have been fully considered but they are not persuasive and are moot in view of the new ground(s) of rejection.

** The relied references including Nowak '846 and Long '381 are directed to an SOI transistor having asymmetric diode properties at the source and drain regions, wherein floating body effect is avoided or reduced.

** Applicant remarked about "product-by-process" claims (at remark page 7) are noted. However, in this case, *the product as claimed* is anticipated by the prior art references.

** Applicant further remarked (at remark pages 8-9) that Nowak (or Long) does not teach "precisely located impurity regions at edges of a trench defined by dielectric layer 35...Figures 1D and 1F of Nowak...that the implantation(s) are performed using a mask 19..., moreover, the implantation(s) are performed over a relatively broad region of the transistor largely coextensive with the source and drain regions...".

In response, again, claims are directed to the product per se, no matter how actually made by process limitations including the use of a mask 19 having only a single edge during implantation, since wherein the impurities of the prior art are located in the semiconductor layer and precisely defined by edges of the gate structure and at edges of a trench formed by a dielectric layer. Indeed, for example, by removing the dielectric layer 14 (as shown in Figure 10 of the present invention), the **claimed** transistor is not patentably different from the transistor of Nowak or Long, wherein the impurities as claimed are thus located at edges of the gate structure.

Regarding implanting over a relatively broad region of the transistor largely coextensive with the source and drain regions, the claimed limitation does not preclude such formation. In other words, the claimed invention does not require structural differences for locations of the source and drain regions and the impurities supplied at edges of the trench. Claimed subject matter, not the specification, is the measure of invention. Limitations in the specification cannot be read into the claims for the purpose of avoiding the prior art. In Re Self, 213 USPQ 1,5 (CCPA 1982); In Re Priest, 199 USPQ 11,15 (CCPA 1978).

Again, it is noted that the claims are still involved to "product by process" claim. However, the claims are directed to the product per se, no matter how actually made by process limitations including "implanting", "diffusion" from "a sidewall within", "angled implantation", "planarizing", "removing", etc.. A "product by process" claim is directed to the product per se, no matter how actually made, *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); In re Marosi et al, 218 USPQ 289; and particularly In re Thorpe, 227 USPQ 964, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an

old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael M. Trinh whose telephone number is (703) 308-2554. The examiner can normally be reached on M-F from 8:30 Am to 4:30 Pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (703) 308-4905. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Oacs-4

Michael Trinh
Primary Examiner